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Description

LOW-VOLTAGE CURVATURE-COMPENSATED BANDGAP REFERENCE

Background of Invention

[0001] 1. Field of the Invention

[0002] The present invention relates to a voltage reference circuit with low sensitivity to temperature, and more specifically, to a low-voltage bandgap reference circuit.

[0003] 2. Description of the Prior Art

[0004] Reference voltage generators are widely used in both analog and digital circuits such as DRAM and flash memories. A bandgap reference (also termed BGR) is a circuit that provides a stable output voltage with low sensitivity to temperature and supply voltage.

[0005] A conventional bandgap reference output is about 1.25 V, which is almost equal to the silicon energy gap measured in electron volts. However, in modern deep-submicron

technology, a voltage of around 1 V is preferred. As such, the conventional bandgap reference is inadequate for current requirements.

[0006] The 1 V minimum supply voltage is constrained by two factors. First, the reference voltage of about 1.25 V exceeds 1 V. Second, low voltage design of proportional-to-absolute-temperature (PTAT) current generation loops is limited by the input common-mode voltage of the amplifier. The effects of these constraints can be reduced by resistive subdivision methods and by using low threshold voltage devices or BiCMOS processes. However, both of these solutions require costly special process technology.

[0007] Bandgap references can be divided into two groups: type-A and type-B. Type-A bandgap references sum voltages of two elements having opposite temperature components. Type-B bandgap references combine the currents of two elements. Both type A and type B bandgap references can be designed to function with a normal supply voltage of greater than 1 V and a sub-1-V supply voltage.

[0008] Fig.1 illustrates a conventional type-A bandgap reference circuit 10. The bandgap reference circuit 10 includes an operational amplifier 12, two transistors M1 and M2, two resistors R1 and R2, and two diodes Q1 and Q2. The

sources of the transistors M1, M2 are connected to a supply voltage V_{DD}. The drain of the transistor M1 is connected to the emitter of the diode Q1 through the resistor R1 and to the positive input of the amplifier 12. Similarly, the drain of the transistor M2 is connected to the emitter of the diode Q2 through the resistor R2 and to the negative input of the amplifier 12. The gates of the transistors M1, M2 are connected to the output of the amplifier 12. In CMOS applications, each diode Q1, Q2 is formed with a parasitic vertical bipolar transistor having a collector and base connected to ground.

[0009] Neglecting base current, the emitter-base voltage of a forward active operation diode can be expressed as:

[0010]
$$V_{EB} = \frac{kT}{q} \ln\left(\frac{I_C}{I_S}\right)$$

(1)

[0011] where:

[0012] k is Boltzmanns constant (1.38×10^{-23} J/K),

[0013] q is the electronic charge (1.6×10^{-19} C),

[0014] T is temperature,

[0015] I_C is the collector current, and

[0016] I_S is the saturation current.

[0017] When the input voltages of the amplifier 12 are forced to be the same, and the size of the diode Q1 is N times that of the diode Q2, the emitter-base voltage difference between diodes Q1 and Q2, ΔV_{EB}, becomes:

[0018]
$$\Delta V_{EB} = V_{EB2} - V_{EB1} = \frac{kT}{q} \ln N \quad (2)$$

[0019] where:

[0020] V_{EB1} is the emitter-base voltage of diode Q1, and

[0021] V_{EB2} is the emitter-base voltage of diode Q2.

[0022] Finally, when the current through resistor R1 is equal to the current through resistor R2 and is set to be PTAT, an output reference voltage, V_{REF}, can be obtained by:

$$V_{REF} = V_{EB2} + \frac{R_2}{R_1} \Delta V_{EB} \equiv V_{REF-COMV}$$

(3)

[0023] where:

[0024] R_1 is the resistance of resistor R1,

[0025] R_2 is the resistance of resistor R2, and

[0026] $V_{REF-CONV}$ is the reference voltage (conventional).

[0027] The emitter-base voltage, V_{EB}, has a negative temperature coefficient of -2mV/°C, while the emitter-base voltage difference, ΔV_{EB}, has a positive temperature coefficient of 0.085 mV/°C. Hence, if a proper ratio of resistances of resistors R1 and R2 is selected, the output reference voltage, V_{REF}, will have low sensitivity to temperature. In general, the supply voltage, V_{DD}, is set to about 3-5 V and the output reference voltage, V_{REF}, is about 1.25 V, as the conventional bandgap circuit 10 cannot be used at a lower voltage such as 1 V.

[0028] Fig.2 illustrates a conventional type-B bandgap reference circuit 20. Elements in Fig.2 having the same reference numbers of those in Fig.1 are the same. The bandgap reference circuit 20 includes an operational amplifier 22; three transistors M1, M2, and M3; four resistors R1, R2, R3, and R4; and two diodes Q1 and Q2 interconnected as illustrated in Fig.2.

[0029] Compared with the type-A circuit 10, the type-B circuit 20 is more suitable for operating with a low supply voltage. Instead of stacking two complementary voltages, the type-B bandgap reference 20 adds two currents with opposite temperature dependencies. In the bandgap reference of Fig.2, the current through the resistor R3 is PTAT. If the resistances of the resistors R1 and R2 are equal, then the current through the MOS transistor M3 mirrored from transistors M1 and M2 can be expressed as:

$$I_{M3} = \frac{1}{R_1}\left(V_{EB2} + \frac{R_1}{R_3}\frac{kT}{q}\ln N\right)$$

(4)

[0030] with the reference voltage being expressed as:

$$V_{REF} = \frac{R_4}{R_1}\left(V_{EB2} + \frac{R_1}{R_3}\frac{kT}{q}\ln N\right) = \frac{R_4}{R_1}\cdot V_{REF-CONV}$$

(5)

[0031] Thus, in the bandgap reference circuit 20 of Fig.2, as ratios of resistances are key, the variations in individual resistances due to process conditions does not greatly affect the reference voltage. In general, the supply voltage,

V_{DD}, is set to about 1.5 V and the output reference voltage, V_{REF}, is about 1.2 V.

[0032] Fig.3 illustrates a conventional type-B bandgap reference circuit 30 capable of sub-1-V operation. Elements in Fig.3 having the same reference numbers of those in Fig.2 are the same. The bandgap reference circuit 30 includes an operational amplifier 32; three transistors M1, M2, and M3; six resistors R1a, R1b, R2a, R2b, R3, and R4; and two diodes Q1 and Q2 interconnected as illustrated in Fig.3. The supply voltage is limited by the input common-mode voltage of the amplifier 32, which must be low enough to ensure that the input pair operate in the saturation region.

[0033] The improvement of low supply voltage realized with the bandgap reference circuit 30 is based on the positions of the input pair of the operational amplifier 32. The established feedback loop produces a PTAT voltage across the resistor R3. The resistance ratio of the resistors R1a and R2a causes the voltage between the supply voltage and the input common voltage of the operational amplifier 32 to become increased. This makes the p-channel input pair operate in the saturation region even when the supply voltage is under 1V. The sub-1-V reference voltage output by the circuit 30 can be expressed as:

[0034] $$V_{REF-SUBV} = \frac{R_4}{R_1}\left(V_{EB2} + \frac{R_1}{R_3}\frac{kT}{q}\ln N\right) = \frac{R_4}{R_1}\cdot V_{REF-CONV}$$

(6)

[0035] which is similar to the circuit 20 of Fig.2. During operation of the circuit 30, the supply voltage, V_{DD}, is set to about 1.0-1.9 V and the output reference voltage, V_{REF}, is about 0.6 V.

[0036] Given the state-of-the-art bandgap reference circuits 10, 20, and 30 described above, it is clear that an improved and inexpensive low-voltage bandgap reference circuit is required.

SUMMARY OF INVENTION

[0037] It is therefore a primary objective of the claimed invention to provide a low-voltage curvature-compensated bandgap reference circuit having low sensitively to temperature.

[0038] Briefly summarized, the claimed invention includes a first bandgap reference unit having an output connected to a first node, a second bandgap reference unit having an output connected to a second node, and a subtractor connecting the first and second bandgap reference units at the first and second nodes. The subtractor comprises a first transistor having a source connected to a first volt-

age, and a drain and a gate both connected to the second node; a second transistor having a source connected to the first voltage, a drain connected to a third node, and a gate connected to the gate of the first transistor; a third transistor having a source connected to a second voltage, and a drain and a gate both connected to the first node; a fourth transistor having a source connected to the second voltage, a drain connected to the third node, and a gate connected to the gate of the third transistor; and an output resistor connected between the third node and to the second voltage.

[0039] It is an advantage of the claimed invention that a temperature insensitive reference voltage of less than 1 volt can be obtained at the third node when the first and second voltages are set appropriately.

[0040] It is a further advantage of the claimed invention that the bandgap reference circuit is compatible with established CMOS technology.

[0041] It is a further advantage of the claimed invention that no low-threshold voltage or BiCMOS devices are required.

[0042] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the

preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0043] Fig.1 is a circuit diagram of a conventional bandgap reference.

[0044] Fig.2 is a circuit diagram of a conventional low-voltage bandgap reference.

[0045] Fig.3 is a circuit diagram of a conventional low-voltage bandgap reference.

[0046] Fig.4 is a graph of base-emitter voltage versus temperature of two diodes of a bandgap reference.

[0047] Fig.5 is a graph of the difference of the diode base-emitter voltages of Fig.4 versus temperature.

[0048] Fig.6 is a graph of a family of output reference voltage curves.

[0049] Fig.7 is a circuit diagram of a low-voltage curvature-compensated bandgap reference circuit according to a first embodiment.

[0050] Fig.8 is a graph of the currents and a reference voltage of the circuit of Fig.7.

[0051] Fig.9 is a schematic diagram of a parasitic vertical NPN CMOS BJT.

[0052] Fig.10 is a circuit diagram of a low-voltage curvature-

compensated bandgap reference circuit according to a second embodiment.

[0053] Fig.11 is a circuit diagram of a low-voltage curvature-compensated bandgap reference circuit according to a third embodiment.

[0054] Fig.12 is a graph of reference voltage versus temperature for the bandgap reference of Fig.11.

[0055] Fig.13 is a graph of minimum supply voltage for the bandgap reference of Fig.11.

DETAILED DESCRIPTION

[0056] As a basis for the explaining the present invention, please refer to Fig.4 and Fig.5. Fig.4 illustrates base-emitter voltage of two diodes Q1, Q2 (discussed later) with respect to temperature. Fig.5 illustrates the difference of the diode base-emitter voltages with respect to temperature. It can be seen that the base-emitter voltage, V_{EB}, has a negative temperature coefficient of about -2 mV/°C with V_{EB}=0.55 V and T=300 K. The difference of the diode base-emitter voltages, ΔV_{EB}, with respect to temperature, as shown in Fig.5, is used in the present invention to produce a PTAT to eliminate the effect of the negative temperature coefficient.

[0057] As a further basis, consider that the output reference volt-

age, V_{REF}, of a conventional bandgap circuit is given by:

[0058]
$$V_{REF} = E_G + V_T(\gamma - \alpha)\left(1 + \ln\frac{T_0}{T}\right)$$

(7)

[0059] where:

[0060] γ is from

$$\mu = CT^{\gamma-4}$$

[0061] defining the average hole mobility in the base,

[0062] α is from

$$I_C = GT^{\alpha}$$

[0063] E_G is the bandgap voltage of silicon,

[0064] T_0 is the temperature in Kelvin where the temperature coefficient of V_{REF} is zero, and

[0065] T is temperature in Kelvin.

[0066] Neglecting the temperature dependence of the bandgap voltage of silicon ,E_G, and differentiating (7) once and twice with respect to temperature yields:

[0067]
$$\frac{\partial V_{REF}}{\partial T} = \frac{k}{q}(\gamma - \alpha)\ln\frac{T_0}{T}$$

(8)

[0068] and

[0069]
$$\frac{\partial}{\partial T}\left(\frac{\partial V_{REF}}{\partial T}\right) = -\frac{k}{q}\frac{(\gamma - \alpha)}{T}$$

(9)

[0070] It should be noted that the term (γ−α) in (9) controls the curvature of the V_{REF} curve of (7). So that if the term (γ−α) is positive then V_{REF} is concave down everywhere, and if the term (γ−α) is negative then V_{REF} is concave up everywhere.

[0071] Referring to Fig.6, illustrating a family of concave up output reference voltage curves according to (7). Fig.6 shows several curves of different zero-reference-temperatures T_0 according to a simulation specifying a bandgap circuit with PNP bipolar transistors of a TSMC 0.25 μm 1P5M process, pure p-type silicon near room temperature, and

γ=1.8 and α=0.

[0072] Please refer to Fig.7 illustrating a low-voltage curvature-compensated bandgap reference circuit 70 according to a first embodiment of the present invention. The bandgap reference circuit 70 is a CMOS circuit, however other implementations are certainly possible. The circuit 70 includes a first bandgap reference unit 72 having an output connected to a first node n1, a second bandgap reference unit 74 having an output connected to a second node n2, and a subtractor 76 connected between the bandgap reference 72, 74. The first bandgap reference unit 72 is a p-channel device that outputs a current I_1, and the second bandgap reference unit 74 is an n-channel device that outputs a current I_2.

[0073] The subtractor 76 includes a first transistor M4 having a source connected to a first voltage V_{DD} and a drain and gate both connected to the second node n2, and a second transistor M5 having a source also connected to the first voltage V_{DD}, a drain connected to a third node n3, and a gate connected to the gate of the first transistor M4. The transistors M4 and M5 and PNP devices. The subtractor 76 further comprises a third transistor M6 having a source connected to ground and a drain and gate both connected

to the first node n1, and a fourth transistor M7 having a source connected to ground, a drain connected to the third node n3, and a gate connected to the gate of the third transistor M6. The transistors M6 and M7 are NPN devices. An output resistor RREF is connected between the third node n3 and ground.

[0074] Please refer to Fig.8 illustrating the currents and reference voltage of the circuit 70 of Fig.7. The currents I_1 and I_2 are both concave up and both have similar curvature when the first and second reference units 72, 74 are designed to have close values of T_0. As can be seen in Fig.8, a fundamental operation of the subtractor 76 is to subtract the smaller current I_1 generated by the first bandgap reference 72 from the larger current I_2 generated by the second bandgap reference 74. The result of this operation is a temperature insensitive and curvature-compensated voltage V_{REF} across the resistor RREF. In addition, Fig.9 illustrates a schematic diagram of a parasitic vertical NPN bipolar junction transistor (BJT) made with standard CMOS processes with a deep n-well, which is one kind of device that can be used to realize the present invention.

[0075] Please refer to Fig.10 illustrating a circuit diagram of a low-voltage curvature-compensated bandgap reference

circuit 100 according to a second embodiment of the present invention. The circuit 100 includes a p-channel bandgap reference unit 102 (similar to the unit 72) and an n-channel bandgap reference unit 104 (similar to the unit 74) mutually connected by the subtractor 76. The circuit 100 can be considered as a more specific embodiment of the circuit 70, and consequently the previous description of the circuit 70 also applies to the circuit 100.

[0076] The p-channel bandgap reference unit 102 is similar to the bandgap reference circuit 20 of Fig.2, and as such, components with same reference numerals are the same. The p-channel bandgap reference unit 102 includes a first operational amplifier 112; a fifth transistor M1 having a source connected to the first voltage V_{DD}, a drain connected to the positive input end of the amplifier 112, and a gate connected to the output end of the amplifier 112; and a sixth transistor M2 having a source connected to the first voltage V_{DD}, a drain connected to the negative input end of the amplifier 112, and a gate connected to the output end of the amplifier 112. The circuit 102 further comprises a first resistor R1 connected between ground and the positive input end of the amplifier 112, a second resistor R2 connected between ground and the negative

input end of the amplifier 112, a first diode Q1 having a collector and base connected to ground and an emitter connected to the positive input end of the amplifier 112 through a third resistor R3, and a second diode Q2 having a collector and base connected to ground and an emitter connected to the positive input end of the amplifier 112. Finally, the circuit 102 comprises a seventh transistor M3 having a source connected to the first voltage V_{DD}, a gate connected to the output end of the amplifier 112, and a drain connected to the first node n1. The transistors M1, M2, M3 and the diodes Q1, Q2 are PNP.

[0077] The n-channel bandgap reference unit 104 is similar to an n-channel version of the bandgap reference circuit 20 of Fig.2. The n-channel bandgap reference unit 104 includes a second operational amplifier 114; an eighth transistor M1 having a source connected to ground, a drain connected to the positive input end of the operational amplifier 114, and a gate connected to the output end of the operational amplifier 114; and a ninth transistor M2 having a source connected to ground, a drain connected to the negative input end of the amplifier 114, and a gate connected to the output end of the amplifier 114. The circuit 104 further comprises a fourth resistor R1 connected

between the first voltage V_{DD} and the positive input end of the amplifier 114, a fifth resistor R2 connected between the first voltage V_{DD} and the negative input end of the amplifier 114, a third diode Q1 having a collector and base connected to the first voltage V_{DD} and an emitter connected to the positive input end of the amplifier 114 through a sixth resistor R3, and a fourth diode Q2 having a collector and base connected to the first voltage V_{DD}, and an emitter connected to the positive input end of the amplifier 114. Finally, the circuit 104 comprises a tenth transistor M3 having a source connected to ground, a gate connected to the output end of the amplifier 114, and a drain connected to the second node n2. The transistors M1, M2, M3 and the diodes Q1, Q2 are NPN.

[0078] From (4), the current produced by the p-channel bandgap reference unit 102 at the node n1 is given by:

[0079]
$$I_1 = \frac{1}{R_1}\left(V_{EB2} + \frac{R_1}{R_3}\frac{kT}{q}\ln N_{PNP}\right) = \frac{V_{REF\_PNP}}{R_1}$$

(10)

[0080] where:

[0081] R_1 is the resistance of the resistor R1,

[0082] R_3 is the resistance of the resistor R3,

[0083] V_{EB2} is the emitter-base voltage of diode Q2,

[0084] N_{PNP} is the ratio of the sizes of diodes Q1 and Q2, and

[0085] V_{REF_PNP} is the voltage at the first node n1.

[0086] Similarly, the current produced by the n-channel bandgap reference unit 104 at the node n2 can be expressed as:

[0087]
$$I_2 = \frac{1}{R_1'}\left(V_{BE2} + \frac{R_1'}{R_3'}\frac{kT}{q}\ln N_{NPN}\right) = \frac{V_{REF\_NPN}}{R_1'} \quad (11)$$

[0088] where:

[0089] R_1 is the resistance of the resistor R1,

[0090] R_3 is the resistance of the resistor R3,

[0091] V_{BE2} is the base-emitter voltage of the diode Q2,

[0092] N_{NPN} is the ratio of the sizes of diodes Q1 and Q2, and

[0093] V_{REF_NPN} is the voltage at the second node n2.

[0094] Then, applied with (7) the difference current $\Delta I = I_2 - I_1$ is:

$$\Delta I = E_G\left(\frac{1}{R_1'} - \frac{1}{R_1}\right) + V_T\left(1 + \ln\frac{T_0}{T}\right)\left(\frac{(\gamma-\alpha)_{NPN}}{R_1'} - \frac{(\gamma-\alpha)_{PNP}}{R_1}\right)$$

(12)

[0095] where:

[0096] γ for NPN circuit 104 is 1.58 for silicon at room temperature, and

[0097] γ for PNP circuit 102 is 1.8 for silicon at room temperature.

[0098] When suitable resistance values for the resistors R1 and R1 are selected, the latter term in (12) can be eliminated. Neglecting the temperature dependence of E_G, ΔI becomes a temperature independent current. Therefore, a temperature independent current is achieved across the resistor RREF, and the corresponding output reference voltage can be expressed as:

$$V_{REF} = R_{REF}(I_2 - I_1) = \frac{R_{REF}}{R_1}\left((V_{BE2} - V_{BE2}) + \left(\frac{1}{R_3'} - \frac{1}{R_3}\right)R_1 \frac{kT}{q} \ln N\right)$$

(13)

[0099] where:

[0100] R_{REF} is the resistance of the resistor RREF, and

[0101] $R_1 = R_1$ and $N_{NPN} = N_{PNP}$.

[0102] By tuning the resistors, close values of T_0 for the bandgap units 102, 104 can be obtained easily. Thus, the bandgap

units 102, 104 produce two currents (I_1 and I_2 respectively) of different magnitudes but similar T_0, such that the subtractor 76 can produce the temperature insensitive voltage V_{REF} at node n3.

[0103] For the second embodiment bandgap reference circuit 100, the minimum supply voltage, $V_{DD(min)}$, is given by:

$$V_{DD(min)} = Max\left[\left(V_{EB2\_PNP} + \left|V_{TP}\right| + 2\cdot\left|V_{DSsat}\right|\right), \left(V_{BE2\_NPN} + V_{TN} + 2V_{DSsat}\right)\right] \quad (14)$$

[0104] where:

[0105] V_{EB2_PNP} is the emitter-base voltage of the diode Q2,

[0106] V_{BE2_NPN} is the base-emitter voltage of the diode Q2,

[0107] V_{TP} is the PNP threshold voltage,

[0108] V_{TN} is the NPN threshold voltage, and

[0109] V_{DSsat} is the drain-source saturation voltage.

[0110] Please refer to Fig.11 illustrating a circuit diagram of a low-voltage curvature-compensated bandgap reference circuit 200 according to a third embodiment of the present invention. The circuit 200 includes a p-channel bandgap reference unit 202 (similar to the units 72, 102) and an n-channel bandgap reference unit 204 (similar to the units 74, 104) mutually connected by the subtractor

76. The circuit 200 can be considered as a more specific embodiment of the circuit 70, and consequently the previous description of the circuit 70 also applies to the circuit 200.

[0111] The p-channel bandgap reference unit 202 is similar to the bandgap reference circuit 30 of Fig.3, and as such, components with same reference numerals are the same. The p-channel bandgap reference unit 202 includes the operational amplifier 112; the transistor M1 having the source connected to the voltage V_{DD}, the drain connected to the positive input end of the amplifier 112 through a seventh resistor R1a, and the gate connected to the output end of the amplifier 112; and the transistor M2 having the source connected to the voltage V_{DD}, the drain connected to the negative input end of the amplifier 112 through an eighth resistor R2a, and the gate connected to the output end of the amplifier 112. The circuit 202 further comprises a ninth resistor R1b connected between ground and the positive input end of the amplifier 112, a tenth resistor R2b connected between ground and the negative input end of the amplifier 112, the diode Q1 with collector and base connected to ground and emitter connected to the drain of the transistor M1 through the third

resistor R3, and the diode Q2 with collector and base connected to ground and emitter connected to the drain of the transistor M2. Finally, the circuit 202 comprises the transistor M3 having the source connected to the voltage V_{DD}, the gate connected to the output end of the amplifier 112, and the drain connected to the first node n1. In the p-channel bandgap reference unit 202, as in the unit 102, the transistors M1, M2, M3 and diodes Q1, Q2 are PNP.

[0112] The n-channel bandgap reference unit 204 is similar to an n-channel version of the bandgap reference circuit 30 of Fig.3. The n-channel bandgap reference unit 204 includes the operational amplifier 114; the transistor M1 having the source connected to ground, the drain connected to the positive input end through an eleventh resistor R1a, and the gate connected to the output end of the amplifier 114; the transistor M2 having the source connected to ground, a drain connected to the negative input end of the amplifier 114 through a twelfth resistor R2a, and a gate connected to the output end of the amplifier 114; a thirteenth resistor R1b connected between the voltage V_{DD} and the positive input end of the amplifier 114; and a fourteenth resistor R2b connected between the voltage V_{DD} and the negative input end of the amplifier 114. The cir-

cuit 204 further comprises the diode Q1 with collector and base connected to the voltage V_{DD} and emitter connected to the drain of the transistor M1 through the resistor R3, and the diode Q2 with collector and base connected to the voltage V_{DD} and emitter connected to the drain of the transistor M2. Finally the circuit includes the transistor M3 having the source connected to ground, the gate connected to the output end of the amplifier 114, and the drain connected to the second node n2. In the n-channel bandgap reference unit 204, as in the unit 104, the transistors M1, M2, M3 and diodes Q1, Q2 are NPN.

[0113] For the third embodiment bandgap reference circuit 200, the minimum supply voltage, $V_{DD(min)}$, is given by:

[0114]
$$V_{DD(\min)} = Max\left[\left(\frac{R_{1b}}{R_{1a}+R_{1b}}V_{EB2\_PNP} + \left|V_{TP}\right| + 2\cdot\left|V_{DSsat}\right|\right), \left(\frac{R'_{1b}}{R'_{1a}+R'_{1b}}V_{EB2\_NPN} + V_{TN} + 2V_{DSsat}\right)\right]$$

(15)

[0115] where:

[0116] R_{1a}, R_{1b}, R_{1a}, and R_{1b} are the resistances of the resistors R1a, R1b, R1a, and R1b, respectively.

[0117] Operation and results of the first, second, and third em-

bodiment circuits 70, 100, 200 are similar. In the third embodiment, equation (13) still applies, however, the value of R_1 is really $R_{1a}+R_{1b} = R_{1a}+R_{1b}$. Generally, the second embodiment circuit 100 is more accurate requiring a supply voltage V_{DD} = 1.5 V, while third embodiment circuit 200 is less accurate but only requires the supply voltage V_{DD} = 0.9 V.

[0118] Fig.12 is a graph of reference voltage versus temperature, and Fig.13 is a graph of minimum supply voltage for the third embodiment bandgap reference circuit 200 of Fig.11. Fig.12 and Fig.13 plot results of a simulation of the circuit 200 which specified TSMC 0.25 μm technology. Fig.12 shows a 10.7 ppm/°C bandgap voltage reference from -10 to 120 °C. Fig.13 shows the minimum supply voltage of 0.9 V.

[0119] While the bandgap reference circuits 70, 100, and 200 were previously described as CMOS circuits, there is no reason why they cannot be implemented with other technologies such as with discrete components, BiCMOS, or emerging semiconductor processes. Furthermore, suitable combinations, where a mix of component types are used, of current or new technologies can also be used to realize the present invention.

[0120] In contrast to the prior art, the present invention provides a curvature-compensated low-voltage bandgap reference having a temperature insensitive reference voltage of less than 1 volt at the third node. Such a circuit can be readily manufactured with established CMOS method, and no low-threshold voltage or BiCMOS devices are required.

[0121] Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

[0122]